Study program: Modern computer technologies

Course title: VHDL Design

Professor/assistant: Miloš B. Stojanović

Type of course: elective

ECTS credits: 6

Pre-requisites: none

Aims of the course:

The aim of the course is to introduce students to and teach them about the basic principles of design and synthesis of integrated circuits using computers. Students are instructed on how to use program packages for design, simulation, synthesis and testing. They will learn how to use the basics of hardware description language VHDL. Instruction is also provided on the design and synthesis of a system of low and mid-level complexity in VHDL, implemented in FPGA.

Learning outcomes:

Once the student has passed the exam, he/she will be able to independently design integrated circuits using a computer.

Syllabus

Theoretical part

Integrated circuit design. Design domains (functional, structural, physical). Levels of modelling and abstraction. Design process. Program packages used for designing. Languages used to describe hardware. VHDL code organization and design styles. Simulation and synthesis of the VHDL code and the role it plays in the design process. Components, packages, libraries. Language structures. Concurrent and sequential codes. Parametric design. Hierarchical design. RTL design.

Practical part

Designing a new project using the Xilinx ISE Design Suite program package, selection of an integrated circuit for synthesis. Design of a source (VHDL) design file, selection of the type of design file. Defining the interface (ports) of the model being designed. Defining the architecture of the module and the time limitation. Test-bench, and generation of the test-bench. A functional simulation. A timing simulation. Designing a testing circuit. Circuit synthesis. Generating a report on synthesis – the RTL diagram. Implementation, and generation of a report on implementation. A report on the pins. Defining the limitations. Generating a configuration file. Connecting a PC to the development system. Configuration of the FPGA circuit. Testing of FPGA circuit.

Literature

1. Milivojević. Z., *Projektovanje pomoću računara,* Punta, Niš, 2003.
2. Volnei A. P., *Circuit Design and Simulation with VHDL*, the MIT Press, Cambridge, 2010.
3. Đorđević. G., *Arhitekture mikrosistema*, Elektronski fakultet Niš, 2009.

Number of active classes			Other forms of teaching:
Lectures: 30	Practical classes: 15	Research work:	

Teaching methods

Combined, interactive classes with solutions offered from practice.

Grading system (maximum 100 points), **grading scale** from 5 to 10: below 51 points grade 5, grade 6 from 51-60 points, grade 7 from 61-70 points, grade 8 from 71-80 points, grade 9 from 81-90 points, grade 10 from 91-100 points.

Pre-exam obligations	**points**	**Final exam**	**points**
activity during theoretical lectures	**10**	written exam	**30**
practical training	**30**	oral exam	
colloquium(s)/seminar papers	**30**		
Sum	**70**	**Sum**	**30**